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INDEX GUIDED VCSEL
AND
METHOD OF FABRICATION

Field of the Invention

This invention relates to vertical cavity surface emitting lasers and, more particularly, to semiconductor lasers which operate reliably at high frequencies.

Background of the Invention

Vertical cavity surface emitting lasers (hereinafter referred to as "VCSELs") have become the dominant light source for optical transmitters used in short-reach local area networks and storage area network applications, in which a multi-mode optical fiber is used for data transmission. VCSELs are low cost micro-cavity devices with high speed, low drive current and low power dissipation, with desirable beam properties that significantly simplify their optical packaging and testing. In order to extend the application of VCSELs to higher speed applications, the VCSEL must be capable of operating reliably at frequencies of up to 10 GHz.

1 Commercial oxide confined VCSELs have been widely
2 deployed in the field. However, due to intrinsic mechanical
3 stress introduced by the oxidation in the VCSEL fabrication,
4 oxide confined VCSELs are not as reliable as, for example,
5 proton (or ion) implanted VCSELs with higher random failure
6 rates. Prior art VCSELs which include an oxide confinement
7 may operate at 10 GHz, but they suffer from poor reliability.
8 Prior art ion implanted VCSELs typically operate at about 1
9 GHz, but are more reliable than VCSELs with oxide confinement.
10 Although certain stress relief methods may be introduced to
11 reduce the random failure rate, the oxidation process is too
12 sensitive to the temperature, materials composition, and gas
13 pressure during device fabrication and, therefore, the oxide
14 confinement process is not a consistent manufacturing process
15 for VCSELs.

16
17 Ion implanted VCSELs are relatively more reliable.
18 However, ion implanted devices do not perform well at higher
19 speeds and, therefore, their applications are limited to data
20 rates around 1 Gbps. The speed of an ion implanted VCSEL is
21 limited by several factors. One factor is the lack of a good
22 index guiding for the optical mode. Another factor is from a
23 size limitation due to a deep implant where the typical
24 implant depth may be more than three microns. Further, the
25 implant has a distribution with a large straggle and a large

1 standard deviation. With a large implant distribution and the
2 poor current confinement of a heavily doped mirror, the size
3 is typically more than 20 microns wherein the speed is limited
4 to less than 2 GHz.

5

6 Therefore, there is a need to develop a reliable high
7 performance VCSEL for high speed optical communications.

8

9 Accordingly, it is an object of the present invention to
10 provide new and improved VCSELs that operate reliably at high
11 frequencies.

12

13 It is another object of the present invention to provide
14 new and improved VCSELs with reduced current leakage and
15 device capacitance.

16

Summary of the Invention

Briefly, to achieve the desired objects of the instant invention in accordance with a preferred embodiment thereof, a reliable high frequency vertical cavity surface emitting laser (VCSEL) is provided. The VCSEL includes a lower distributed Bragg reflector, an active region positioned on the lower distributed Bragg reflector, and an upper distributed Bragg reflector positioned on the active region. A cylindrical volume is etched from the upper distributed Bragg reflector so as to define a mesa with a substantially vertical side wall concentrically surrounded by the cylindrical volume. An isolation trench is etched in a lower surface of the cylindrical volume concentric with the mesa. An implant region is formed in the cylindrical volume, including a portion of the side wall of the mesa and a portion of the upper distributed Bragg reflector below the lower surface of the cylindrical volume. The cylindrical volume is filled with a dielectric or insulating material to planarize the VCSEL for further isolation and passivation. Electrical contacts are coupled to opposite sides of the active region for supplying operating current thereto.

The desired objects of the instant invention are further achieved through a novel method of fabricating a high

1 frequency vertical cavity surface emitting laser. The method
2 includes providing a lower distributed Bragg reflector on a
3 substrate, an active region on the lower distributed Bragg
4 reflector, and an upper distributed Bragg reflector on the
5 active region. The method also includes etching a cylindrical
6 volume from the upper distributed Bragg reflector to define a
7 mesa with a substantially vertical side wall, the cylindrical
8 volume extending into the upper distributed Bragg reflector to
9 a lower surface adjacent the active region and etching an
10 isolation trench in the lower surface of the cylindrical
11 volume concentric with the mesa and extending through the
12 active region. The method further includes a step of
13 implanting a portion of the side wall of the mesa and the
14 lower surface of the cylindrical volume and planarizing the
15 upper distributed Bragg reflector. Finally, coupling n and p
16 electrical contacts are coupled to opposite sides of the
17 active region for supplying operating current thereto.

1 Brief Description of the Drawings

2

3 The foregoing and further and more specific objects and
4 advantages of the instant invention will become readily
5 apparent to those skilled in the art from the following
6 detailed description of a preferred embodiment thereof taken
7 in conjunction with the following drawings:

8

9 FIG. 1 is a simplified sectional view of a high speed
10 vertical cavity surface emitting laser in accordance with the
11 present invention; and

12

13 FIG. 2 is a simplified top plan view of the high speed
14 vertical cavity surface emitting laser illustrated in FIG. 1.

Detailed Description of the Drawings

Turning now to FIG. 1, a simplified sectional view of a vertical cavity surface emitting laser (VCSEL) 10 is illustrated. Also, FIG. 2 illustrates a top plan view of complete VCSEL 10, which may be referred to in addition to FIG. 1 throughout this discussion. VCSEL 10 includes a substrate 12 which may be, for example, some convenient single crystal semiconductor material, such as gallium arsenide (GaAs) or the like. As is well known in the art, in most instances a thin buffer layer 14 of the same material is provided to ensure a smooth crystalline surface for further growth processes. Layer 14 is considered part of the substrate in this disclosure. A lower mirror stack or distributed Bragg reflector (DBR) 16 is grown on the upper surface of substrate 12. An active region 18 which, as is known in the art, may include cladding regions or the like (not shown) on opposite sides, is grown on the upper surface of DBR 16. An upper mirror stack or distributed Bragg reflector (DBR) 20 is grown on the upper surface of active region 18. As is understood by those skilled in the art, the various layers and/or regions described above are generally grown epitaxially in a well known continuous procedure. Also, the chosen deposition technique is not meant to limit the scope of the invention. For example, in this embodiment, the

1 basic structure of VCSEL 10 is formed using metallorganic
2 chemical vapor deposition (MOCVD). However, it will be
3 understood that VCSEL 10 may be formed using chemical vapor
4 deposition, sputtering, molecular beam epitaxy, or
5 combinations thereof. Further, although a single VCSEL is
6 illustrated, generally, a plurality of VCSELs are deposited or
7 formed in blanket layers over an entire wafer so that a large
8 number of VCSELs are fabricated simultaneously.

9

10 In this embodiment, substrate 12 includes gallium
11 arsenide (GaAs). However, the choice of substrate material
12 and the material included in active region 18 generally
13 depends on a desired wavelength of operation which in this
14 embodiment is between approximately 0.7 μm to 1.0 μm . It will
15 also be understood that the wavelength range from 0.7 μm to
16 1.0 μm is typically used in optical communication
17 applications, such as fiber optical networks. However, other
18 wavelength ranges may be suitable for a given application.

19

20 As is understood in the art, DBRs 16 and 20 include a
21 stack of alternate layers of materials wherein each adjacent
22 layer has a different index of refraction. For example, DBRs
23 16 and 20 in this embodiment include alternate layers of
24 semiconductor material, such as alternate layers of an alloy

1 of AlGaAs, with different proportions of material to change
2 the index of refraction, or alternate layers of aluminum
3 arsenide (AlAs) and gallium arsenide (GaAs). It will be
4 understood that DBRs 16 and 20 may include other suitable
5 reflective materials that are stacked alternately between a
6 high and a low index of refraction. Further, in the preferred
7 embodiment, each layer in DBRs 16 and 20 have thicknesses
8 approximately equal to one quarter of the wavelength of
9 operation to provide a desired reflective property. Also,
10 while lower DBR 16 is illustrated as being doped for n-type
11 conductivity and upper DBR 20 is illustrated as being doped
12 for p-type conductivity, it will be understood that the
13 conductivities could be changed and the present formation is
14 only for purposes of explanation.

15

16 Active region 18 may include from one to a plurality of
17 quantum structure layers with a band gap wavelength wherein
18 each quantum structure layer emits light at the wavelength of
19 operation. For example, active region 18 may include layers
20 of aluminum gallium arsenide (AlGaAs), gallium arsenide
21 (GaAs), or indium gallium arsenide (InGaAs). It will be
22 understood that active region 18 may include quantum wells or
23 other device structures with suitable light emission
24 properties, such as quantum dots or similar device structures.
25 The quantum structure layers, quantum wells; quantum dots,

1 etc. are spaced within active region 18 in a well known manner
2 to provide the desired light generation.

3

4 Once the basic structure, including lower DBR 16, active
5 region 18, and upper DBR 20 is completed, an etching process
6 is performed in a ring-shaped area to remove a cylindrical
7 volume 24 from upper DBR 20 to define a mesa 25 in upper DBR
8 20. The etching process continues through DBR 20 to within a
9 few mirror pairs of active region 18. Further, the etching
10 process is performed so that more mirror pairs remain near the
11 base of mesa 25 and less mirror pairs remain as the lateral
12 distance from mesa 25 (within volume 24) increases. That is,
13 the angle between the vertical side of mesa 25 and the
14 surrounding upper surface of DBR 20 is greater than ninety
15 degrees. This 'rounding' of the mesa corner reduces the
16 stress effect within the crystalline material and improves
17 reliability. Also, mesa 25 is formed to provide an optical
18 and current confinement region.

19

20 Once volume 24 is etched as described above, a second
21 etch step is performed within concentric cylindrical volume 24
22 to form an isolation trench 28, spaced from mesa 25, that
23 extends through the remaining mirror pairs in upper DBR 20,
24 active region 18, and into lower DBR 16. Isolation trench 28
25 (and volume 24) extends concentrically around mesa 25 and is

1 included to reduce current leakage and device capacitance.
2 The trench etching step can be performed before or after an
3 implant step, which is described in detail below, depending
4 upon the convenience and continuity of the various steps. For
5 example, a first etch followed immediately by a second etch
6 may be more convenient than interspersing an implant step
7 between.

8

9 With at least the mesa defining etching process
10 completed, a proton implant process is performed on the side
11 wall of mesa 25 and the remaining DBR mirror pairs immediately
12 under volume 24 to form implant area 30. Generally, the
13 mirror pairs remaining adjacent mesa 25 are sufficient so that
14 proton implant area 30 adjacent mesa 25 is close but does not
15 extend into active region 18. However, as the lower surface
16 of cylindrical volume 24 extends laterally a greater distance
17 from mesa 25, e.g. adjacent isolation trench 28, implant area
18 30 gradually begins to extend into active region 18. In a
19 specific embodiment, the implant is from one to four DBR pairs
20 of layers, or approximately 0.1 to 0.5um. This was achieved
21 using an implant energy in a range of approximately 30 to 70
22 KV with proton implant.

23

24 The etching of cylindrical volume 24, including the side
25 wall of mesa 25, causes crystalline damage with dangling bonds

1 and defects at the etch surface which in turn causes unwanted
2 carrier trapping and non-radiative carrier recombination.
3 However, implant region 30 has a high resistance to electrical
4 current flow so that electrical current will not flow in the
5 implanted area and, therefore, non-radiative carrier
6 recombination cannot occur in the damaged crystalline etched
7 portions. Also, because implant region is on the surface and
8 relatively thin, deep implants are not required and the entire
9 implant process can be very accurately controlled. Further,
10 since the implant is adjacent the surface (very shallow) a
11 less complicated proton implant can be used. Here it should
12 be noted that most prior art implants in VCSELs were made
13 through most or even the entire upper mirror stack, thereby
14 requiring the lighter ion implants. Implant region 30 is
15 provided to stop or prevent current/carrier recombination
16 activated defect propagation from the etched side wall of mesa
17 25 into active area 18 to substantially improve the
18 reliability of VCSEL 10. Thus, a combination of etching and
19 implant procedures are used to fabricate VCSEL 10 with all the
20 advantages of both processes and none or few of the
21 disadvantages.

22
23 VCSEL 10 is then planarized using benzocyclobutene (BCB)
24 dielectric (CycloteneTM from Dow) or some convenient polyimide
25 materials 32 to provide for better metallization coverage and

1 to reduce device capacitance for high speed operation. In
2 addition, BCB is a low- k dielectric material and further helps
3 reduce the VCSEL parasitic capacitance. A p-contact metal ring
4 34 is concentrically deposited on the upper surface of mesa 25
5 and an n-contact metal layer 35 is applied to the rear surface
6 (lower surface in FIG. 1) of substrate 12. An insulating and
7 passivating coating 38 of some convenient silicon-oxide-
8 nitride silicon nitride, or the like is applied to the upper
9 surfaces of VCSEL 10. An opening is provided in coating 38 at
10 least over a portion of p-contact metal ring 34. A top bond-
11 pad metal layer 40 is deposited in contact with the exposed
12 portion of p-contact metal ring 34 and extending over a
13 convenient portion of coating 38.

14

15 Thus, a reliable high performance VCSEL for high
16 speed optical communications is disclosed. The new and
17 improved VCSELs are constructed to operate reliably at high
18 frequencies and with reduced current leakage and device
19 capacitance. Basically, the new and improved VCSELs are
20 fabricated using a convenient mixture of etching and shallow
21 implanting to provide a device having all of the advantages of
22 both processes while eliminating substantially all of the
23 disadvantages.

1 While the steps of the fabrication method have been
2 described, and will be claimed, in a specific order, it will
3 be clear to those skilled in the art that various steps and
4 procedures may be performed in different orders. It is
5 intended, therefore, that the specific order described or
6 claimed for the various fabrication steps does not in any way
7 limit the invention and any variations in order that still
8 come within the scope of the invention are intended to be
9 covered in the claims.

10

11 Various changes and modifications to the embodiments
12 herein chosen for purposes of illustration will readily occur
13 to those skilled in the art. To the extent that such
14 modifications and variations do not depart from the spirit of
15 the invention, they are intended to be included within the
16 scope thereof which is assessed only by a fair interpretation
17 of the following claims.

18

19 Having fully described the invention in such clear and
20 concise terms as to enable those skilled in the art to
21 understand and practice the same, the invention claimed is: